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IN THE CLAIMS

1. (previously amended) An integrated circuit substrate comprising:
a first surface adapted for receiving a series of aligned layers during the creation
of the integrated circuit, the first surface having no layers formed thereon,
and
5 a second surface disposed substantially opposite the first surface, the second
surface having no layers formed thereon and at least one alignment mark
formed thereon, the at least one alignment mark adapted for aligning the
series of aligned layers one to another during the creation of the integrated
circuit.
2. (original) The substrate of claim 1 wherein the second surface is divided into a
first half and a second half, with one alignment mark in each of the first half and
the second half.
3. (original) The substrate of claim 1 wherein the second surface is divided into
quadrants, with one alignment mark in each of the quadrants.
4. (original) The substrate of claim 1 wherein the at least one alignment mark is
printed on the second surface.
5. (original) The substrate of claim 1 wherein the at least one alignment mark is
recessed into the second surface.
6. (original) The substrate of claim 1 wherein the at least one alignment mark
comprises geometric shapes in a pattern.
7. (cancelled)
8. (cancelled)
9. (cancelled)
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11. (cancelled)
12. (cancelled)
13. (cancelled)
14. (cancelled)
15. (cancelled)

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- 16. (cancelled)
- 17. (cancelled)
- 18. (cancelled)
- 19. (cancelled)
- 20. (cancelled)